Computer and Measurement Simulation of a New Digital Receiver Operating Directly at Millimeter-Wave Frequencies

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***Abstract*—A novel digital millimetric receiver (DMR) scheme is introduced. Using a six-port phase/frequency discriminator (SPD) in conjunction with a digital signal processor (DSP), the receiver performs various PSK and QAM demodulations directly at microwave and millimeter-wave frequencies. An important feature of the new DMR is that hardware imperfections such as phase/amplitude imbalance are readily eliminated by a simple calibration procedure. The concept is proved through computer simulation and measurements at 26.5 GHz. This receiver scheme is proposed for small/medium capacity digital terminals typically found in various wireless communication networks.**

I. Introduction

Due to the increasing demand of wireless communications, there have been persistent efforts to simplify the microwave/mm-wave digital transceiver structures to bring down their size and cost. Such efforts have been intensified recently due to fast emerging demands for personal communication services (PCS). Among various choices, the direct (homodyne) transceiver architecture is an effective way to significantly reduce transceiver complexity and cost. Both direct transmitter [1]–[3] and receiver [4]–[6] for different digital modulations using different circuits ranging from hybrid microwave integrated circuit (HMIC) to monolithic microwave integrated circuit (MMIC) technologies have been reported. All these direct transceivers have one point in common: a quadrature hybrid network (I-Q network). It is well known that, as the frequency increases, the corresponding wave-length decreases proportionally, and it is therefore more difficult to obtain a quadrature hybrid with acceptable phase and amplitude accuracy. This is particularly true when the frequency goes beyond microwave into the millimeter-wave band. Although additional circuits can be introduced to compensate phase and amplitude imbalances of the I-Q hybrid [7], [8], this method is obviously cumbersome, and the long-term stability of such circuits is questionable.

As a result of the latest advancement in digital integrated circuit technologies, there is noticeable interest to replace analog circuit functions with their digital implementations [10], [11]. This generally brings down the cost and increases the stability as well as the flexibility of the electronic systems; particularly when DSP's are used. The processing power of the latest DSP is reported to have reached 2 bops [12] which makes it possible to realize some very complex algorithms at high speed. Certain types of receivers sample signals in the IF band and implement the demodulation using DSP's [13]. These receivers, however, still retain all the microwave parts found in the conventional heterodyne receiver. For the design of microwave transceivers, it appears to be more reasonable to simplify the microwave circuit configuration at the expense of more complicated digital circuits, such as to make a better trade-off to reduce the cost and increase the yield of MMIC's.

Six-port theory was first developed in the 70's as a new means of accurate automated microwave network analysis [14], [15]. The vector ratio of the incident waves at two input ports can be calculated using the output power readings at the remaining four ports. In doing this there is no need of down-converting the signal to an IF to make phase comparison. A very interesting feature of the six-port is its ability to eliminate measurement errors introduced by hardware imperfections by a suitable calibration procedure [22]. After more than twenty years of development the six-port technology has become highly sophisticated and some commercial products are now available on the market [16]. In addition, recent progress in MMIC and MHMIC six-ports [17], [18] renders such circuits better accessible for widespread commercial applications.

In this paper, we describe a novel concept of direct digital receiver, in which a six-port replaces the I-Q quadrature hybrid as the phase detector. The block diagram of the new scheme is shown in Fig. 1. The demodulation is performed directly at microwave/mm-wave frequencies by a six-port discriminator (SPD) instead of the I-Q demodulator found in conventional digital receivers. This SPD is capable of detecting relative amplitude, phase and frequency of the received signal with respect to the local oscillator. A DSP unit executes computations necessary to perform the required demodulation in addition to carrier and clock recoveries using algorithms that are already available [32]–[36]. Such a receiver benefits from all the advantages of six-port technology: First, the fabrication requirements of the hardware can be greatly eased. An auxiliary calibration algorithm [19] performs the required six-port calibration from the received signal itself, monitors

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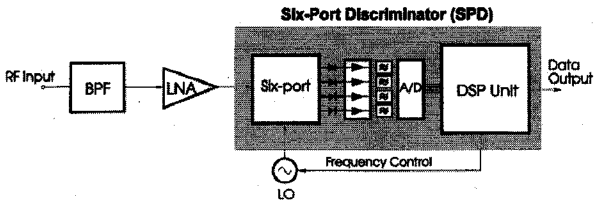


Fig. 1. Block diagram of the new digital millimetric receiver (DMR) with the six-port discriminator (SPD).

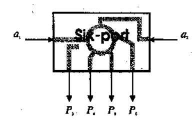


Fig. 2. A six-port function as microwave vector voltmeter as a_1/a_2 is calculated from P_i's.

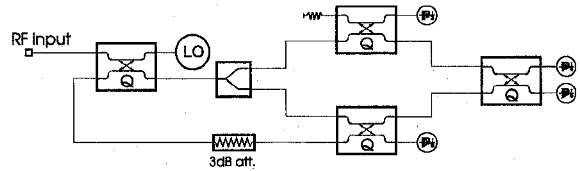


Fig. 3. Block diagram of the six-port model used in simulation of SPD.

the real-time operation and updates the calibration coefficients as temperature and/or some other circuit parameters vary. This makes it possible to realize a direct millimeter wave digital receiver without stringent fabrication requirements; Second, the presence of a DSP provides a great flexibility to the receiver function: Switching between different modulations can be done by simply altering the software routines thereby avoiding hardware reconfiguration. Both differential and coherent detections are possible [24]. Furthermore, the demodulation and decoding functions can be combined together to further enhance the receiver system integration; Third, the proposed six-port receiver possesses unique properties such as: a) Immunity to image frequency and adjacent channel interferences, so that the specification of the channel bandpass filter can be relaxed; b) The six-port receiver allows variation in input power level. The dynamic range of the receiver is mainly a function of the A/D converter resolution. c) Wide band operation is also possible by the use of a wide-band six-port design. After all, the maximum data transmission rate is limited by the A/D converter and DSP. The data throughput is expected to increase as the speed of the DSP escalates in time.

II. Six-Port Discriminator (SPD)

Previously reported six-port applications are mostly focused on microwave measurements such as network analysis [20] and parameter extraction [21]. These measurements involve only coherent signals, i.e., the incident and reflected waves of the microwave networks are generated from the same signal source. Consider the case of a six-port used as a microwave vector voltmeter, the complex ratio of the two input signals a_1 and a_2 in Fig. 2 can be obtained as follows

$$\vec{A} = |A|e^{j\theta} = \frac{\vec{a}_1}{\vec{a}_2} = \frac{\sum_{i=3}^{6}(a_i + jb_i)P_i}{\sum_{i=3}^{6} c_i P_i} \tag{1}$$

where constants a_i, b_i, and c_i's are calibration parameters that depict the specific six-port and can be deduced from a popular two-step calibration procedure [22].

To extend the scope of the six-port a little further, we define the two incident waves to be at different frequencies as follows

$$\vec{a}_1 = |a_1| \cdot e^{j(2\pi f_1 t + \phi_1)} \tag{2}$$

$$\vec{a}_2 = |a_2| \cdot e^{j(2\pi f_2 t + \phi_2)}. \tag{3}$$

Suppose the frequencies f_1 and f_2 are close enough to each other such that the difference in calibration coefficients is negligible for the six-port, the measured complex ratio $\vec{A}$ will become a rotating vector in the complex plane

$$\vec{A} = |A| \cdot e^{j\theta(t)} = |A| \cdot e^{j(2\pi(f_1 - f_2)t + \phi_1 - \phi_2)}. \tag{4}$$

Therefore, the frequency difference $\Delta f = f_1 - f_2$ can be readily obtained from the derivative of $\theta(t)$

$$\Delta f = \frac{\theta(t_2) - \theta(t_1)}{t_2 - t_1} \tag{5}$$

where the time interval between two samples $\Delta t = t_2 - t_1$ is properly chosen for best accuracy. It is to be noted that the sign of Δf is a direct indication of relative position of f_1 and f_2. In this way, the so-called six-port phase/frequency discriminator (SPD) [23] is capable of dealing with all basic receiver functions which are traditionally carried out by I-Q hybrids.

III. Computer Simulation: Performance of SPD Versus I-Q Demodulator

The obstacles preventing conventional I-Q receiver from direct operation at higher frequencies are mainly [25]: 1) Phase imbalance due to circuit imperfections and reflections; 2) Amplitude imbalance due to I-Q circuit, gain imbalance of the two mixer branches, etc., and, 3) DC offset of the I and Q channels. It is recognized that the new SPD can largely overcome such drawbacks. This will be demonstrated through a series of simulation and analysis in the following sections.

A. Circuit Model of Six-Port

A six-port circuit originally designed as a reflectometer is adopted here for simulation purposes. The block diagram of the circuit is shown in Fig. 3. It can be seen that the six-port consists of I-Q hybrids, an in-phase power divider and interconnecting transmission lines. These components are characterized by S-parameters, so that the hardware imperfections can be readily taken into account. A commercial

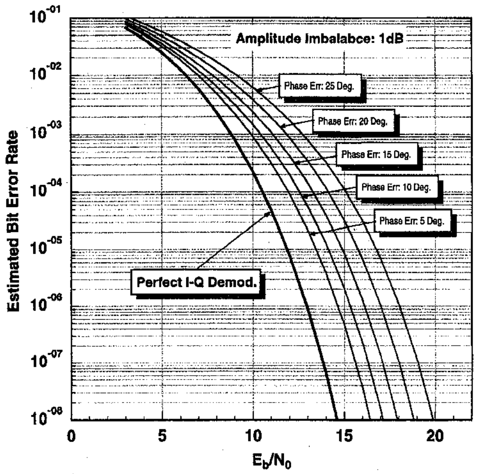
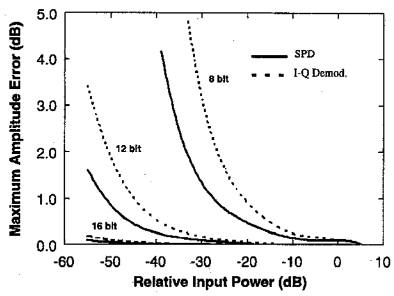
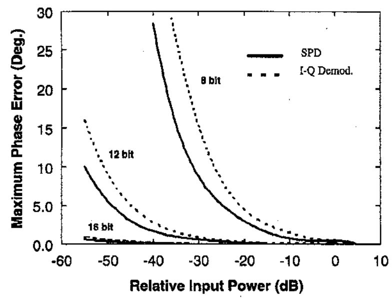


Fig. 4. BER performance of a QPSK receiver in the presence of amplitude and phase imbalance of the I-Q demodulator.



(a)



(b)

Fig. 5. Maximum amp/phase errors versus input power level of SPD and I-Q demodulator.

microwave simulator (MDS[1]) was used to analyze the network. In all the simulations, a real calibration procedure was performed to obtain the corresponding calibration coefficients. Both the simulation and the analysis are performed to compare the SPD to a standard I-Q demodulator operating at the same mm-wave frequency.

B. Degradation of Receiver Performance Due to the Hardware Imperfections

Taking bit error rate (BER) as a straightforward measurement of the receiver performance, for a perfect digital receiver, the only factor affecting performance is noise. The degradation in performance due to various nonideal factors such as hardware imperfections, synchronization errors and interferences can be regarded as equivalent to loss in signal to noise ratio (SNR or E_b/N_0). In order to demonstrate the advantages of using SPD over the conventional I-Q hybrid, simulations have been made for a standard heterodyne QPSK receiver. The transmitter was considered perfect and the phase/amplitude imbalances were introduced in the I-Q demodulator. Fig. 4 shows the BER as a function of E_b/N_0 in the presence of different order of amplitude and phase imbalances. The simulated transmission data rate was 10 Mb/s. The roll-off factor of the raised-cosine band-limit filter was 0.35. It is illustrated that the BER increases with the imbalance. The equivalent E_b/N_0 loss is approximately 1.5 dB, 2.1 dB, 2.9 dB, and 3.7 dB for phase imbalances of 5, 10, 15, and 20 degrees, respectively, at 10^{-4} BER threshold. This E_b/N_0 loss becomes as large as 4.6 dB when the phase imbalance reaches 25 degrees. It is expected that the higher level modulation schemes such as 8PSK and 16QAM are even more sensitive to such imbalances. In some circumstances, the amplitude imbalance between I-Q branches is larger than 1 dB. Therefore in order to maintain a reasonable performance of the receiver, it is absolutely necessary to find an effective way to counter these adverse effects.

[1] Trade Mark of Hewlett Packard.

C. Operating Dynamic Range as a Function of the ADC Resolution

In a conventional heterodyne digital receiver it is generally required that the input level of the I-Q demodulator be kept constant by using an IF automatic gain control (AGC) circuit. However, this becomes more difficult at microwave frequencies. One feature of the six-port direct digital receiver is its tolerance to input signal level variation. Therefore the expensive microwave AGC amplifier is not required. The difference between the maximum and minimum signal levels, while maintaining a given BER margin for a specific modulation, can be defined as the operating dynamic range of the receiver. The minimum detectable signal level depends on the resolution of the A/D converters. On the other hand, an I-Q demodulator also allows variable input signal if the same A/D converters and DSP are used. Fig. 5 illustrates the amplitude and phase errors of SPD and I-Q demodulator as functions of input signal level for 8 bit, 12 bit, and 16 bit A/D converters, respectively. It is obvious that a high resolution A/D converter not only extends the dynamic range but also abates the gain requirement of the preceding low noise amplifier. Meanwhile, the maximum acceptable input level is determined by the saturation point of the power detectors or channel DC amplifier/ADC input limits. Therefore it is concluded that a 50 dB of nominal dynamic range can be readily achieved for QPSK reception using a 16 bit ADC. In most applications it will be more interesting to increase the sensitivity of the SPD to facilitate the LNA design. It is also observed that SPD offers better accuracy than a digitized I-Q demodulator in all cases. For example, from Fig. 5, at a relative input power level of -25 dB, the SPD has maximum amplitude and phase error of 0.8 dB and 5 degrees,

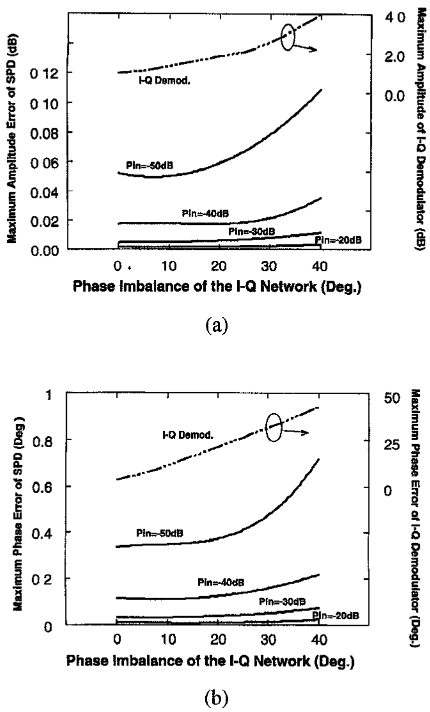


Fig. 6. Accuracy of SPD and I-Q demodulator as functions of imbalances of quadrature hybrid (16 bit ADC).

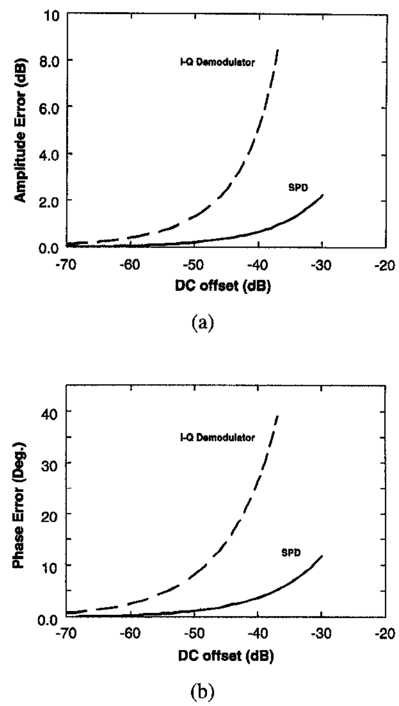


Fig. 7. Accuracy of the SPD and the I-Q demodulator versus DC offset.

respectively when a 8bit ADC is used, while these errors are 1.7 dB and 8 degrees for the I-Q demodulator, respectively.

D. Accuracy of SPD in the Presence of Quadrature Imbalances

The SPD itself can be built up by quadrature hybrids and power dividers or other suitable circuits for phase dispersal. None of these components are perfect. The six-port calibration procedure is to extract the network parameters and eliminate errors from the final measurement results. As a result of noise, the limited resolution of A/D converters and so on, there will still be residual phase and amplitude errors. A statistical simulation has been accomplished to compare the residual errors of SPD with an I-Q hybrid. Random phase and amplitude errors are assigned to each component in the SPD (Fig. 3), and the parameters are random at maximum tolerances for all the components. Consequently, the overall performance of the SPD is the worst possible case at the corresponding error level. Fig. 6 shows the simulation results. An 1-dB amplitude imbalance is presented in all cases. The SPD has 16 bit resolution and the I-Q demodulator uses perfect A/D conversion in the simulation. It is clearly shown that the SPD is very powerful in countering hardware imperfections: in the phase imbalance range of 0 to 40 degrees with the relative input level as low as −50 dB, the maximum residual amplitude and phase errors of SPD are only 0.1 dB and 0.7 degrees, respectively. Therefore it is concluded that the residual error can be considered negligible over the whole dynamic range of the SPD. In contrast, for I-Q demodulators, the errors are directly proportional to hardware errors, i.e. an amp/phase error of 1 dB/25° of the I-Q hardware will result in an error of 2.0 dB in amplitude and 25 degree error in phase, respectively. Although the excellent accuracy of SPD will be degraded somehow in a real receiver due to other factors that have not yet been considered in the simulation such as imperfect calibration and noise, the conclusion that the SPD presents an accuracy several orders superior than I-Q demodulator is still valid. This is confirmed by the measurement simulation.

E. Effect of DC Offset on SPD Accuracy

Fundamentally, the diodes in the SPD operate in a different fashion to their I-Q demodulator counterparts. In an I-Q demodulator the mixers behave like multipliers as the diodes act as nonlinear devices. In a SPD the diodes act as power detectors, and the emphasis is on linearity of the response. Consequently while at least a balanced diode pair must be used for the minimum specifications in an I-Q demodulator, a simple single Schottky diode detector is generally sufficient for a SPD.

The DC offset is primarily introduced by the diode detectors and the attached DC amplifiers, and its value is usually a function of temperature. A computer simulation reveals that, in the case of random offset, the SPD doesn't offer better accuracy than the I-Q demodulator. However, in situations where the offsets of all the channels are moving in the same direction, which is the actual case in single-chip IC's, the SPD comes up with a much greater accuracy.

Fig. 7 displays the phase and amplitude errors as functions of the DC offset. The DC offset is defined as relative to the maximum output voltage of each channel. When the DC offset is at −40 dB, the SPD maintains a minimum acceptable amplitude error of 0.6 dB and a phase error of 3 degrees, while the I-Q demodulator has disastrous 5 dB/26 degrees amplitude/phase errors, respectively. Both amplitude and phase errors are more pronounced for the I-Q demodulator when the DC offset goes beyond −50 dB. Evidently the SPD is

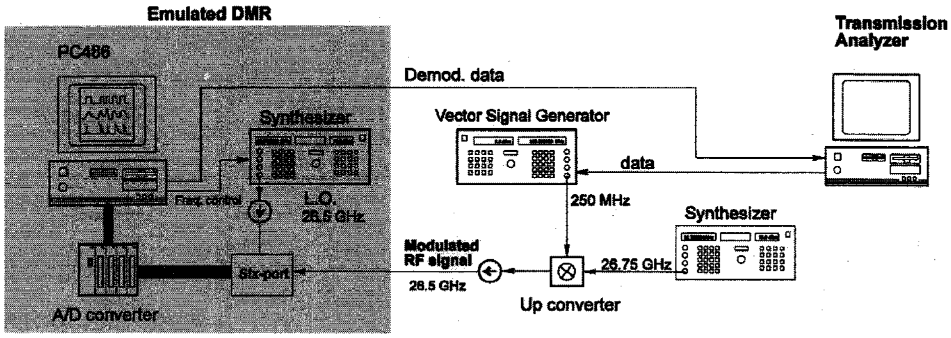


Fig. 8. Test setup for measurement simulation of the new DMR operating at 26.5 Hz.

much less sensitive to the DC offset than its I-Q demodulator counterpart.

F. Effect of Adjacent Channel Interferences

It makes common sense to use filters for most digital receivers to separate the signal from unwanted noise and interferences. While performance degradation caused by inband noise and interferences is inevitable, the SPD possesses unique immunity to out-of-band noise and interferences: For a single diode detector, let us suppose the lowpass filters have stopped all the high frequency components, thus the interference acts only on the DC output. This DC component can be seen as an equivalent DC offset of the DC amplifier. As has already been concluded in the previous section, the I-Q demodulator is more vulnerable to such interferences.

G. Bit Error Rate (BER) Performance

Bit error rate is the ultimate indication of performance of a digital receiver. A statistical computer simulation model was established to help to predict the BER performance of the DMR for various types of modulations. The simulation takes into account several error sources in the real operation, such as phase noise of the local oscillator, resolution of the A/D converter and white noise introduced in diode detectors/DC amplifiers. The results are presented in Fig. 10 together with the measured simulation results.

IV. Measurement Simulation of the DMR

Measurement simulations are also performed. Fig. 8 illustrates the measurement setup. A HP8782B vector signal generator produces the desired modulated signal at an intermediate frequency (250 MHz). Then a upconverter brings this IF signal up to 26.5 GHz and an isolator separates the transmitter from the receiver. There is no filter inserted to suppress the LO and image signal leakage. The variation of the signal level is accomplished by control of the output level of the vector signal generator which has over 160 dB of output level range. No additional bandpass filter is inserted between the transmitter and the receiver. In the SPD, a PC486 with a 16 bit plug-in A/D data acquisition board executes the DSP algorithms. The SPD is constructed using discrete coaxial components for the six-port configuration of Fig. 3. The 3 dB quadrature couplers have ± 1.7 dB of amplitude imbalance, $\pm 10^\circ$ of phase imbalance and a minimum isolation of 14 dB. The in-phase power divider has ± 0.6 dB of amplitude imbalance, and $\pm 4^\circ$ of phase imbalance.

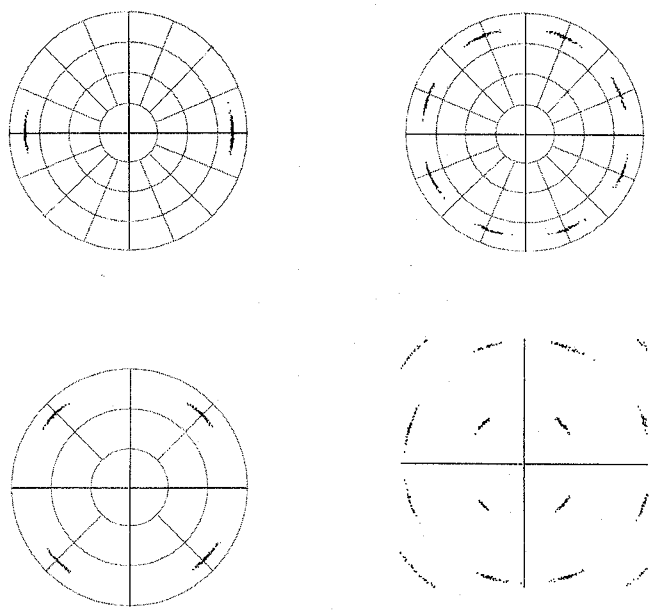


Fig. 9. Sampled constellation diagram of different modulations measured at 26.5 GHz by SPD.

The receiver LO power was about -1.5 dBm for all the measurements. A second PC486 was used as a transmission analyzer for BER tests.

A. Constellation Diagram

Fig. 9 illustrates the measured constellation diagrams of BPSK, QPSK, 8PSK, and 16QAM sampled by the SPD. It clearly proves the efficacy of the SPD in the correction of circuit imbalances. Neither the imbalances of the quadrature couplers nor the LO leakage impose noticeable distortion to the measured constellations. The phase spread in the constellation diagram is due to the phase noise of the oscillators, residual frequency difference and slow sample acquisition time.

It is also noticed that due to the absence of the bandpass filter at the output of transmitter, the LO component in the transmitted spectrum is more than 20 dB higher than the desired signal when the output level of the IF vector signal generator is decreased. Even in this case the observed

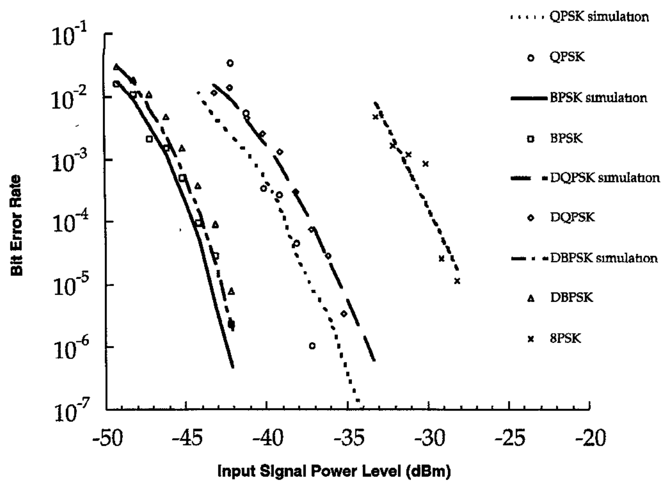


Fig. 10. Measured and simulated BER performance of the SPD for various PSK modulations.

constellation diagram does not appear to be distorted, which reflects the power of the SPD in countering out-of-band interferences.

B. Bit Error Rate Measurements

Demodulation algorithms have been developed for both differential and coherent PSK modulations. The phase recovery for coherent detection is achieved by a simple DSP algorithm. This feature is a better alternative to the more difficult conventional hardware phase tracking directly at microwave/mm wave frequencies.

The measured BER for coherent and differential BPSK, QPSK demodulations are compared with the computer simulation results. Fig. 10 shows the measured and calculated BER versus the input power level. It can be seen that, as anticipated, the coherent reception is better than the differential reception and the BPSK requires minimum energy to be detected. The input power level is about -44.5 dB and -39 dBm for BPSK and QPSK demodulations, respectively, when the BER is 10^{-4}. It is also found that the measurement results are general in agreement with the computer simulations. The poorer agreement in the QPSK results is attributed to a unknown measurement error.

It must be mentioned that these measurements are meant to be "proof of concept" of the new receiver scheme as the transmission data rate was only in the order of several Kb/s due to equipment limitations. Thus it is primarily the ADC resolution, instead of noise, that determines the minimum detectable signal level. On the other hand, the SPD used in the measurements is far from being optimum for receiver applications. Significant improvements in sensitivity can be expected from an optimized design of the SPD.

V. Conclusion

A novel six-port direct digital receiver is presented, and it is found to be rugged to hardware imperfections that normally prevent conventional I-Q receivers from direct operation in microwave/mm wave bands. Computer simulation and measurements at 26.5 GHz validate the new receiver scheme. This work outlines a cost-effective alternative to the conventional heterodyne receiver with the following advantages: 1) High yield of circuit due to decreased fabrication requirements. 2) Low power consumption due to simplicity of the whole receiver and lower LO power demand. 3) Flexibility to switch between different modulation schemes. 4) Less stringent band-pass filter requirements. And 5) The maximum data rate heavily depends on the speed of the DSP unit and A/D converter.

It must be mentioned that although the work described in this paper focuses on mm-wave applications, the DMR can be readily adaptable to lower frequency bands such as the UHF band.

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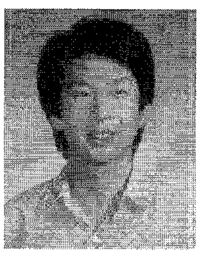

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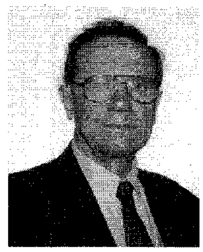

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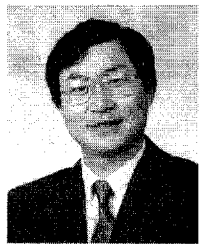

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